

Abstract of Disclosure

A delay line unit of a delay locked loop (DLL) circuit, includes a first delay line having a plurality of first unit delays, each first unit delay having a first delay; a second delay line having a plurality of second unit delays, each second unit delay having a second delay; and a third delay line having a plurality of third unit delays, each third unit delay having a third delay, wherein the first delay is shorter than the second delay, and the second delay is shorter than the third delay.